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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,939	JEONG, JAE GOAN	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) *4-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 1 is rejected under 3 5 U.S. C. 102(e) as being anticipated by Gardner et al., (US 6,077,748).

Gardner et al., in related text (Col. 3, Line 20-Col. 5, Line 39) and figures (Fig. 2A-2J) disclose a device isolation film 66 formed on a semiconductor substrate 10, the device isolation film 66 having a groove that exposes a portion of the semiconductor substrate 10 defining an active region and having a substantially vertical profile with respect to the exposed portion of the semiconductor substrate 10; a gate electrode structure formed in a central portion of the active region of the semiconductor substrate 10 and separated from the device isolation film 66, wherein the gate electrode structure further comprises: a stacked structure of a gate oxide film 68, a first gate electrode 70 and a second electrode 82, an oxide/nitride layer 84 formed on a side wall of the first gate electrode 70, and nitride spacers 84 formed on a side wall of the device isolation film 66; lightly doped drain (LDD) regions 76 formed in the active region of the semiconductor substrate 10 on both sides of the gate electrode structure; source/drain regions 86 formed in the active region of the semiconductor substrate 10 on both sides of the gate electrode

structure, and second and third insulating films 78/80 filling and plananizing the space above the active region and between the gate electrode structure and the device isolation film 66.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitani (US 6,018,185) in view of Gardner et al., (US 6,077,748).

Mitani et al., in related text (Col. 7, Line. 63-Col. 9, Line. 29) and figures (Fig. 2A-2G) disclose a transistor comprising: a device isolation film 104 formed on a semiconductor substrate 101, the device isolation film 104 having a groove that exposes a portion of the semiconductor substrate 101 defining an active region and having a substantially vertical profile with respect to the exposed portion of the semiconductor substrate 101; a gate electrode structure formed in a central portion of the active region of the semiconductor substrate 101 and separated from the device isolation film 104, wherein the gate electrode structure further comprises: a stacked structure of a gate insulation film 106, a first gate electrode 107 and a second electrode 107, an oxide layer 109 formed on a side wall of the first gate electrode 107, and nitride spacers 109 formed on the oxide layer 109 (See Col. 17, Line 67-Col. 18, Line 3 and Fig. 9D) on the sidewall of the first gate electrode 107 and on a side wall of the device isolation film 104; lightly doped drain (LDD) regions 110 formed in the active region of the semiconductor substrate 101 on both

sides of the gate electrode structure; source/drain regions 110 formed in the active region of the semiconductor substrate 101 on both sides of the gate electrode structure; and second and third insulating films 111/112 filling and plananizing the space above the active region and between the gate electrode structure and the device isolation film 104.

Mitani et al. fails to expressly mention the gate insulation comprises silicon oxide.

Gardner et al., in related text (Col. 3, Line 20-Col. 5, Line 39) and figures (Fig. 2A-2J) disclose a device isolation film 66 formed on a semiconductor substrate 10, the device isolation film 66 having a groove that exposes a portion of the semiconductor substrate 10 defining an active region and having a substantially vertical profile with respect to the exposed portion of the semiconductor substrate 10; a gate electrode structure formed in a central portion of the active region of the semiconductor substrate 10 and separated from the device isolation film 66, wherein the gate electrode structure further comprises: a stacked structure of a gate oxide film 68, a first gate electrode 70 and a second electrode 82, an oxide/nitride layer 84 formed on a side wall of the first gate electrode 70, and nitride spacers 84 formed on a side wall of the device isolation film 66; lightly doped drain (LDD) regions 76 formed in the active region of the semiconductor substrate 10 on both sides of the gate electrode structure; source/drain regions 86 formed in the active region of the semiconductor substrate 10 on both sides of the gate electrode structure, and second and third insulating films 78/80 filling and plananizing the space above the active region and between the gate electrode structure and the device isolation film 66.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for using the insulation materials as taught by Gardner et al., within the general skill of

a worker in the art, to select a known material on the basis of its suitability for its intended use is a matter of obvious design choice.

In re claim 2, Mitani et al disclose the vertical profile of the device isolation film is modified near the junction of the device isolation film and the semiconductor substrate such that the device isolation film has a substantially rounded profile (Figs. 2E-2F).

In re claim 3, Mitani et al disclose a hard mask layer 108 is formed on the gate electrode (Figs. 2E-2F).

Response to Arguments

3. Applicant's arguments filed 08/18/03 have been fully considered but they are not persuasive.

It is argued, at page 5 of the remarks, that Mitani fails to anticipate the present invention because "Mitani does not teach or even suggest a stacked structure of the first and the second gate electrode, or the oxide film formed on the first electrode". Mitani et al., in related text (Col. 7, Line. 63-Col. 9, Line. 29) and figures (Fig. 2A-2G) disclose the gate electrode structure comprises: a stacked structure of a gate insulation film 106, a first gate electrode 107 and a second electrode 107, an oxide layer 109 formed on a side wall of the first gate electrode 107, and nitride spacers 109 formed on the oxide layer 109 (See Col. 17, Line 67-Col. 18, Line 3 and Fig. 9D) on the sidewall of the first gate electrode 107. It would have been obvious to one of ordinary skill in the art at the time the invention was made to consider the gate electrode 107 is

formed as two sequentially first and second gate electrode composed of the same material since separating what was once one layer, into many layers, involves only routine skill in the art.

In response to Applicant's argument on page 6 that "the side-wall gate insulation film 109 is formed on the side wall of the entire gate portion". Note that the side-wall gate insulation film 109 is not only formed on the side-wall of first gate electrode 107 but also formed on the side wall of the entire gate portion.

In response to Applicant's argument on page 6 that the second and third insulation films 111/112 planarize the entire surface. Note that the entire surface is formed above the active region and between the first gate electrode and the isolation film. Therefore, second and third insulating films 111/112 filling and plananizing the space above the active region and between the gate electrode structure and the device isolation film 104.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (703) 305-0391. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm.
If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms., can be reached on (703) 308-4910.

DV

David Vu

David Nelms
Supervisory Patent Examiner
Technology Center 2800